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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/784,070	02/16/2001	Per Anders Holmberg	032559-089	4889

27045 7590 04/06/2004

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EXAMINER	
GROSS, KENNETH A	

ART UNIT	PAPER NUMBER
2122	8

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/784,070	Applicant(s) HOLMBERG ET AL.	
	Examiner Kenneth A Gross	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-55 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-55 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 6, 11, 25, and 46 are objected to because of the following informalities: In regard to Claim 6, the term "in that" on line 3 should be deleted. In regard to Claim 11, the comma on line 2, after the term "timer", should be removed. In regard to Claim 25, a comma should be placed after the term "restart" on line 3. In regard to Claim 46, the term "data are" on line 2, should be replaced with "data is". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-55 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, Claims 1, 30, 48, and 52 and child claims recite the term "part entities" which is unclear. Claim 2 defines "part entities" as "an individual variable/record, instructions of a program routine, or instructions of a basic block". However, the term "part entities" in relation to a load module is not known. What exactly is a part entity? Is it a section, or part, of a load module? Claim 6 recites "selecting part entities of a load module of both types of data", however, there is only a "first type of data" mentioned previously in the Claim. What are the "both types of data" being implied in this Claim. Claim 25 recites "a second algorithm for modifying said allocation data at a later occasion". The term "a later occasion" is vague and

indefinite, and does not specifically point out what "a later occasion" is. Is a later occasion a different time then a software start, restart, or change? If a later occasion is during the time when the program is currently running, then is it possible to run a data allocation during program execution? A change of wording is requested, such as "a second algorithm for modifying said allocation data during all other occasions". Claim 39 recites "measuring the time period of said performance characteristics measurement". Does this imply measuring how long it takes to perform the measurement of performance characteristics? Claim 39 further recites "calculating a normalized rate". It is not clear what a normalized rate is, nor why it is being performed during this particular step. What function does the "normalized rate" have with respect to parent Claim 30? Claim 46 recites "after larger reallocations" which is indefinite. What quantity, specifically, is being referred to when the term "larger allocations" is presented? Claim 20 claims to be dependent on Claim 14, however, Claim 14 makes no reference to a link table. Claim 20 is being interpreted to be dependent on Claim 18. Claim 26 claims to be dependent on Claim 21, however, Claim 21 makes no reference to a first algorithm. Claim 26 is being interpreted to be dependent on Claim 25.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5-8, 10, 14, 21-28, 30-32, 34-37, and 43-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Spear et al. (U.S. Patent Number 6,003,115).

In regard to Claim 1, Spear teaches: (a) a processor (Figure 1, item 120); (b) a first RAM (Figure 1, item 110); (c) a second RAM (Column 2, lines 25-28); (d) memory allocation means for allocation of data of a load module of the second memory to first memory, said load module composing variable/record and/or instruction data (Column 4, lines 33-34 and lines 39-43); (e) an execution profiling section for providing execution data concerning behavior of programs executed, wherein operation of said means for memory allocation is software run-time updated based on said execution data, said execution profiling section in turn comprising at least one means for measuring the performance characteristics of part entities of the load module (Column 4, lines 39-50); (f) whereby said memory allocation means is arranged for allocation of selected part entities of said load module to said first memory (Column 4, lines 33-34).

In regard to Claim 2, Spear teaches that part entities are program instructions (Column 4, lines 33-34).

In regard to Claim 3, Spear teaches that the execution profiling section is arranged to select programs according to internal information of an operating system (Column 3, lines 11-19).

In regard to Claim 5, the examiner takes official notice that choosing the programs that are largest in size first is obvious, since optimization of a program can reduce a program's size.

In regard to Claim 6, Spear teaches measuring the performance of an instruction data, and selecting part entities based on these measurements (Column 4, lines 41-50).

In regard to Claim 7, Spear teaches measuring the number of accesses to part entities (Column 7, lines 10-13).

In regard to Claim 8, Spear teaches measuring the number of read accesses to part entities (Column 7, lines 16-18).

In regard to Claim 10, Spear teaches a counter that keeps track of the number of times part entities have been accessed (Column 7, lines 10-13).

In regard to Claim 14, the examiner takes official notice that code instrumentation is well known in the art for determining a count of code access and execution.

In regard to Claim 21, Spear teaches a bus that connects the processor to the memory (Figure 1, item 126).

In regard to Claim 22, Spear teaches a first memory incorporated on a processor chip (Column 2, lines 8-10).

In regard to Claim 23, Spear teaches a first SRAM memory (Figure 1, item 114).

In regard to Claim 24, Spear teaches a third first level cache memory and that the first memory constitutes a second level cache memory (Column 2, lines 8-12).

In regard to Claim 25, Spear teaches a first algorithm for modifying said allocation data upon start of software (Column 4, lines 46-48).

In regard to Claim 26, Claim 26 contains a limitation that has already been addressed in the rejection of Claim 5, and Claim 26 is rejected for the same reasons as Claim 5.

In regard to Claim 27, the examiner takes official notice that saving variable information, where the variables are pointers, means saving reference data, since the pointers contain references to memory addresses.

In regard to Claim 28, Spear teaches a combined memory for storing variables, instructions, and tables (Column 1, lines 35-38).

In regard to Claim 46, the examiner takes official notice that disk defragmentation, or packing data, is a well-known utility to pack data spread out over a memory, and thus reduce access time to the data.

Claim 47 contains a limitation that has already been addressed in the rejection of Claim 1, and Claim 47 is rejected for the same reason as the similar limitation in Claim 1.

Claims 30-32, 34-37, and 43-45 are method Claims which correspond with system Claims 1-3, 5-8, 27, 25, and 26, respectively, and are rejected for the same reasons as Claims 1-3, 5-8, 27, 25, and 26, respectively, where Spear teaches a method carried out by said system of Claim 1 (Column 67, lines 9-28).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9, 12, 15, 17, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spear et al. (U.S. Patent Number 6,003,115) in view of Grimsrud et al. (U.S. Patent Number 5,890,205).

In regard to Claim 9, Spear teaches the system of Claim 1, but does not teach that the performance characteristics comprise means for measuring waiting time for access to part

entities of said load module. Grimsrud, however, does teach profiling access time to a block of memory (Column 4, lines 36-42). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to build the system of Claim 1, as taught by Spear, where the performance characteristics comprise means for measuring waiting time for access to part entities of said load module, as taught by Grimsrud, since this allows optimization based on memory load times.

Claims 12, 15, and 17 contain limitations that have already been addressed in the rejection of Claims 10, 14, and 16, respectively, and Claims 12, 13, 15, and 17 are rejected for the same reasons as Claims 10, 14, and 16, respectively.

Claim 38 is a method Claim that corresponds with system Claim 9 and is rejected for the same reasons as Claim 9, where Spear teaches a method carried out by said system of Claim 9 (Column 67, lines 9-28).

8. Claims 11, 13, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spear et al. (U.S. Patent Number 6,003,115) in view of Berry et al. (U.S. Patent Number 6,662,358).

In regard to Claim 11, Spear teaches the system of Claim 10, but does not teach that the execution profiling section includes a timer for calibration of measured performance characteristics. Berry, however, does teach the use of a time for profile data calibration (Column 29, lines 55-67 and Column 30, lines 1-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to build the system of Claim 10, as taught by Spear, where the execution profiling section includes a timer for calibration of measured

performance characteristics, as taught by Berry, since this allows for updated matching of data based on the timer.

Claim 13 contains imitations that have already been addressed in the rejection of Claim 11, and is rejected for the same reasons as Claim 11.

In regard to Claim 16, Spear teaches the system of Claim 7, but does not teach that the means for measuring the number of accesses is done in an emulator or virtual machine. Berry, however, does teach using a VM to execute a program being profiled (Column 6, lines 61-67 and Column 7, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to build the system of Claim 7, where the means for measuring the number of accesses is done in an emulator or virtual machine, since this allows the running program to be abstracted and executable on any platform.

9. Claims 18-20, 40, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spear et al. (U.S. Patent Number 6,003,115) in view of Zucker (U.S. Patent Number 5,991,871).

In regard to Claim 18, Spear teaches the system of Claim 1, but does not teach that the memory allocation means is arranged to read a link table. Zucker, however, does teach a means for memory allocation reading a link table (Column 24, lines 22-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to build the system of Claim 1, as taught by Spear, where the memory allocation means is arranged to read a link table, as taught by Zucker, since this allows a link table to be considered when performing memory allocation.

In regard to Claim 19, Spear and Zucker teach the system of Claim 18, and Spear does not teach that part of the link table is allocated to said first memory. Zucker, however, does teach

allocating a link table to a first memory (Column 24, lines 22-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to build the system of Claim 18, as taught by Spear and Zucker, where part of the link table is allocated to said first memory, as taught by Zucker, since this allows the link table to be stored and accessed on the first memory.

In regard to Claim 20, the examiner takes official notice that a link table that supports run-time linking is an obvious feature of some link tables since this allows binding of code only to the specific files that need them during runtime.

Claims 40 and 41 are method Claims which correspond with system Claims 18 and 20, respectively, and are rejected for the same reasons as Claims 18 and 20, respectively, where Spear teaches a method carried out by said system of Claims 18 and 20 (Column 67, lines 9-28).

10. Claims 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spear et al. (U.S. Patent Number 6,003,115) in view of Balser (U.S. Patent Number 3,775,756).

In regard to Claim 29, Spear teaches the system of Claim 1, but does not teach a split memory comprised of at least two of variables or records, instructions, or tables. Balser, however, does teach this type of split memory (Column 1, lines 56-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to build the system of Claim 1, as taught by Spear, where the memory is a split memory comprised of instructions and variable or table data, as taught by Balser, since this allows better organization of memory.

11. Claims 4, 33, 42, and 48-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spear et al. (U.S. Patent Number 6,003,115) in view of Vange et al. (U.S. Patent Number 6,390,922).

In regard to Claim 4, Spear teaches the system of Claim 3, but does not teach that the internal information comprises information about the priority of a program. Vange, however, does teach optimizing high priority programs (Column 2, lines 8-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to build the system of Claim 3, as taught by Spear, where the internal information comprises information about the priority of a program, as taught by Vange, since high priority programs should be optimized, since it is of greater importance.

In regard to Claim 42, Spear teaches the method of Claim 30, but does not teach that the step of modification favors allocation of data having the highest measured performance importance per time unit to said first memory. Vange, however, does teach optimizing high priority programs (Column 2, lines 8-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to run the method of Claim 30, as taught by Spear, where the step of modification favors allocation of data having the highest measured performance importance per time unit to said first memory, as taught by Vange, since high priority programs should be optimized, since it is of greater importance.

Claim 33 is a method Claim that corresponds with system Claim 4 and is rejected for the same reasons as Claim 4, where Spear teaches a method carried out by said system of Claim 4 (Column 67, lines 9-28).

Claim 48 contains limitations that have already been addressed in the rejection of Claims 1 and 3, and Claim 48 is rejected for the same reasons as Claims 1 and 3. Claims 49-51 contain limitations that have already been addressed in the rejections of Claims 2, 4, and 5, respectively, and are rejected for the same reasons as Claims 2, 4, and 5, respectively.

Claims 52-55 are method Claim that correspond with system Claims 48-51 and are rejected for the same reasons as Claims 48-51, where Spear teaches a method carried out by said system of Claim 48 (Column 67, lines 9-28).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A Gross whose telephone number is (703) 305-0542. The examiner can normally be reached on Mon-Fri 7:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KAG

TUAN DAM
SUPERVISORY PATENT EXAMINER